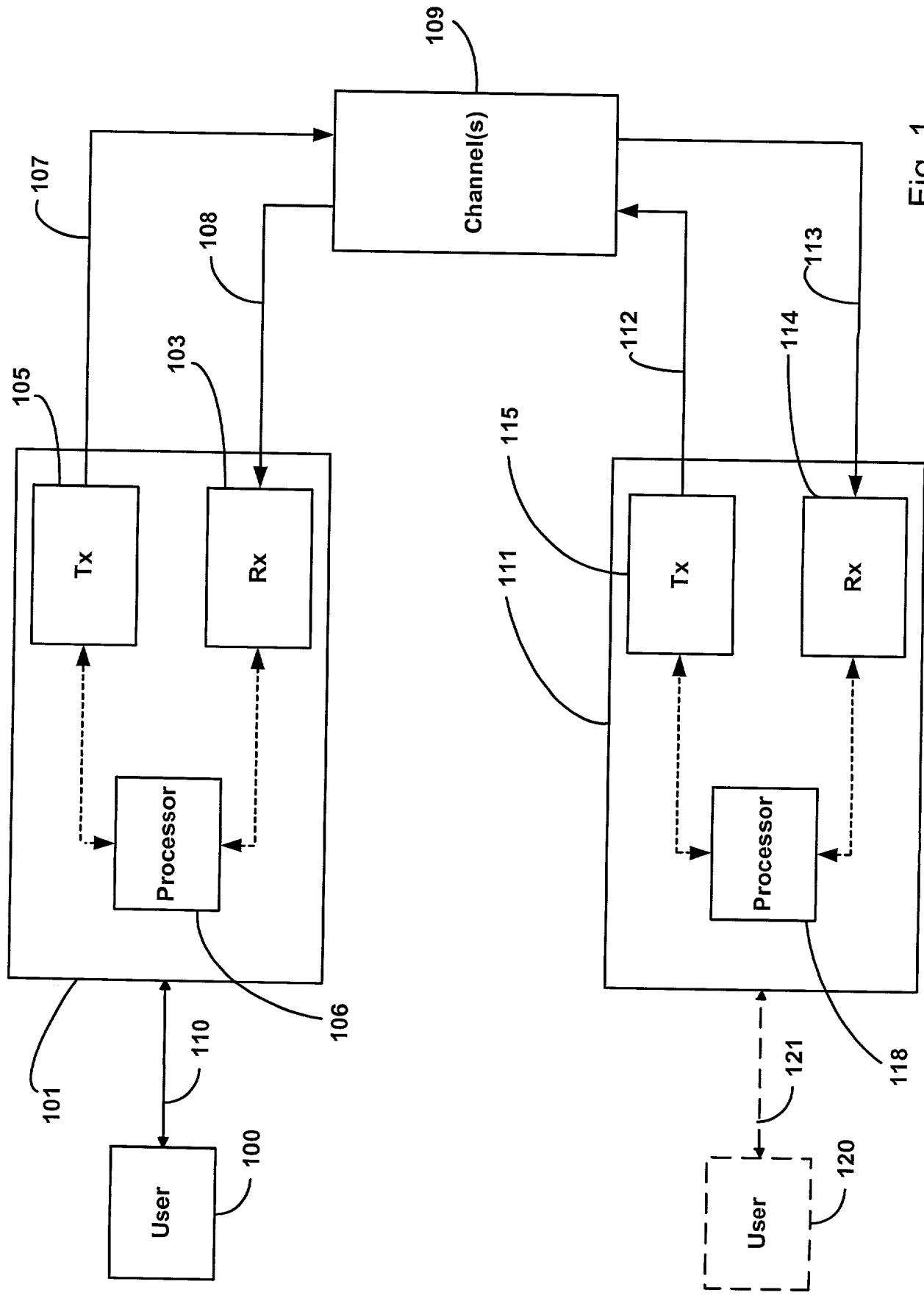


Figure 1 is a block diagram of a communication system 100. The system 100 includes a User 101, a first communication device 105, a second communication device 111, and a Channel(s) 109. The User 101 is connected to the first communication device 105 via a bidirectional arrow 110. The first communication device 105 includes a Processor 103, a Transmitter (Tx) 107, and a Receiver (Rx) 108. The second communication device 111 includes a Processor 115, a Transmitter (Tx) 112, and a Receiver (Rx) 113. The first communication device 105 is connected to the Channel(s) 109 via a bidirectional arrow 106. The second communication device 111 is connected to the Channel(s) 109 via a bidirectional arrow 114. The Channel(s) 109 is connected to the second communication device 111 via a bidirectional arrow 118. The User 101 is shown in a dashed box 120, indicating it is optional or external to the core system.



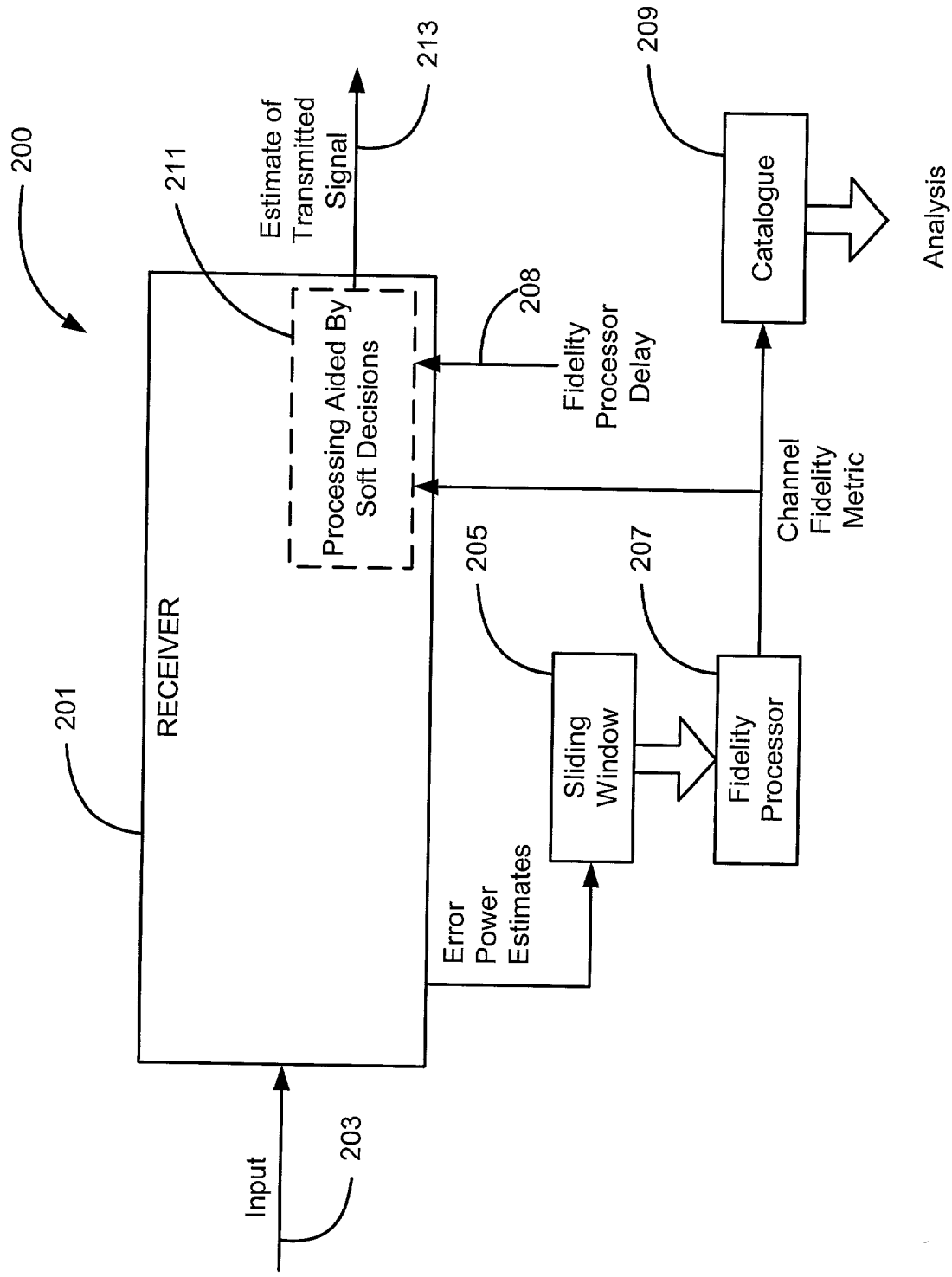


Fig. 2

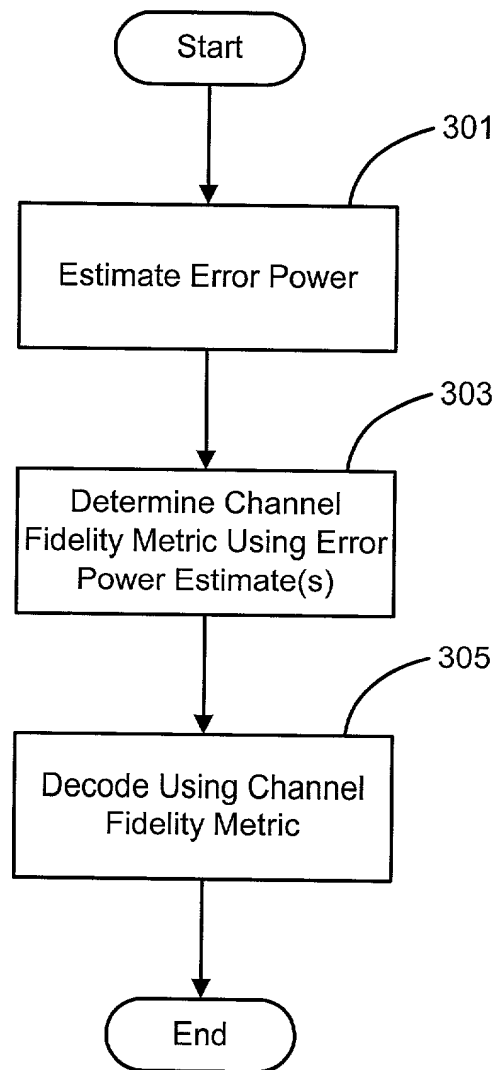


Fig. 3

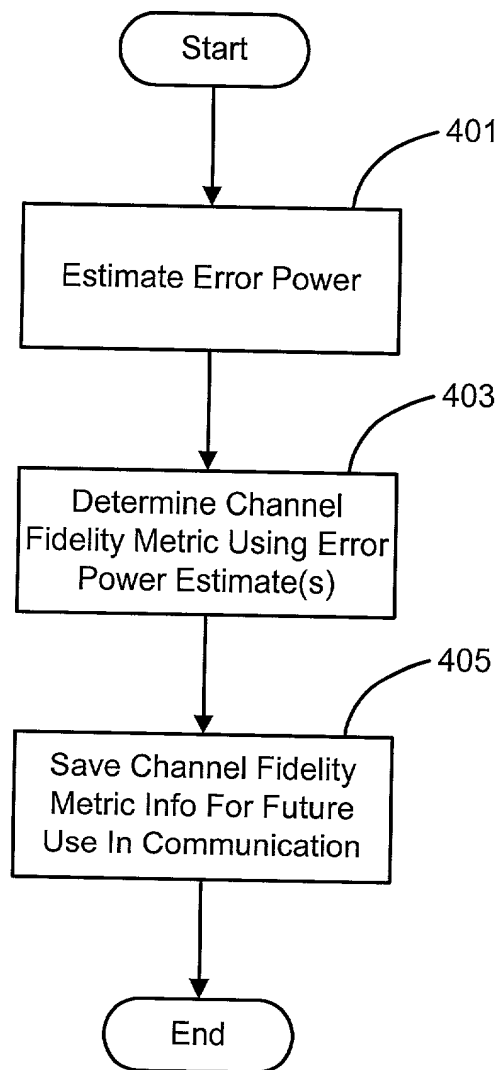


Fig. 4

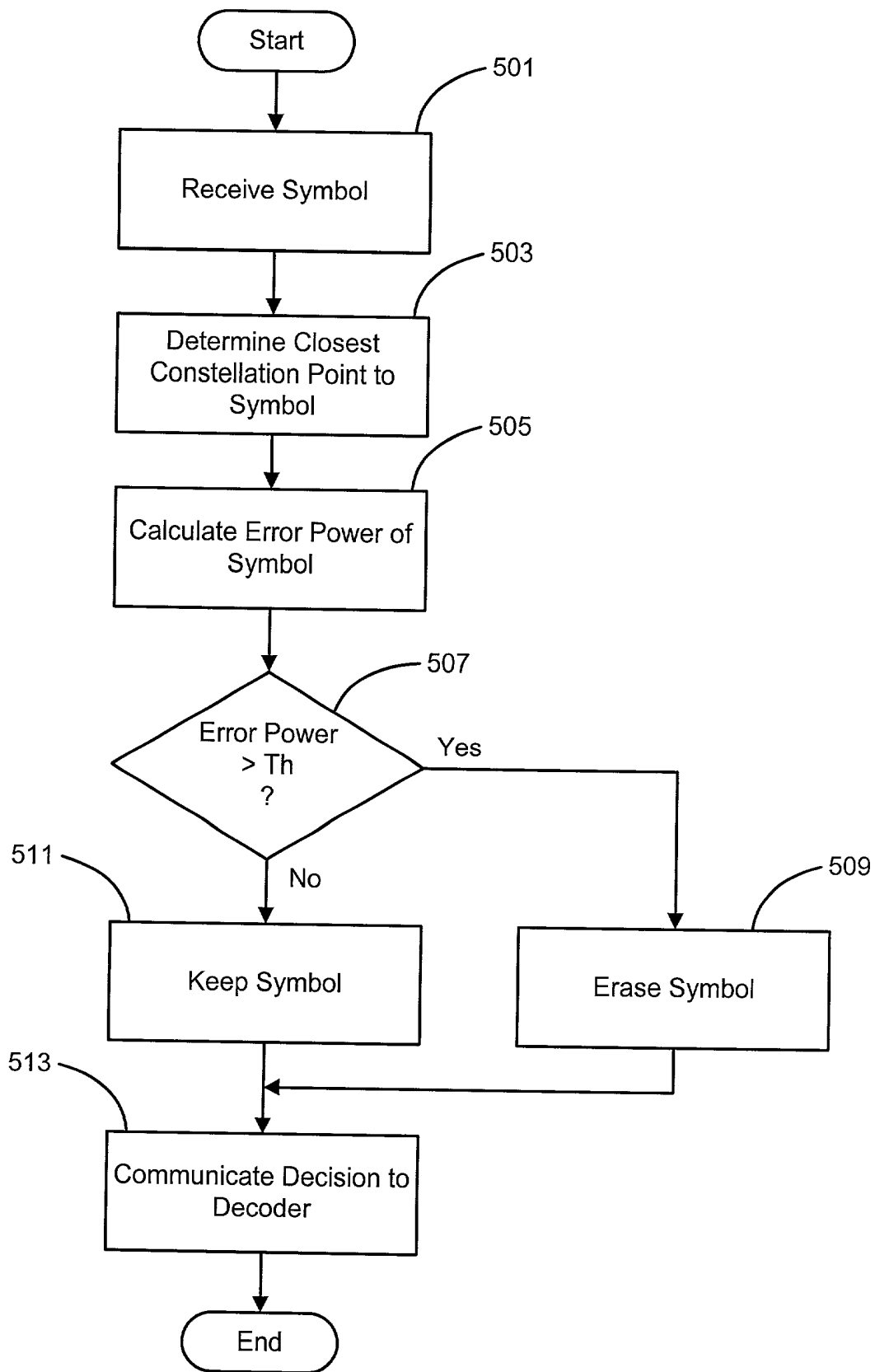


Fig. 5

Fig. 6 is a block diagram of a receiver system 600. The receiver system 600 includes an input 603, a slicer 605, a Reed-Solomon decoder 619, and a data output 621. The slicer 605 is connected to the input 603 and the Reed-Solomon decoder 619. The Reed-Solomon decoder 619 is connected to the data output 621. The receiver system 600 also includes an error power estimate block 607, a 7 tap delay line 609, and a fidelity processor 611. The error power estimate block 607 is connected to the slicer 605 and the fidelity processor 611. The 7 tap delay line 609 is connected to the error power estimate block 607 and the fidelity processor 611. The fidelity processor 611 is connected to the Reed-Solomon decoder 619 and the data output 621. The fidelity processor 611 also includes a channel fidelity metric block 613 and a channel degraded block 615. The channel fidelity metric block 613 is connected to the error power estimate block 607 and the channel degraded block 615. The channel degraded block 615 is connected to the Reed-Solomon decoder 619 and the data output 621. The channel degraded block 615 also includes a delay of 4 symbols.

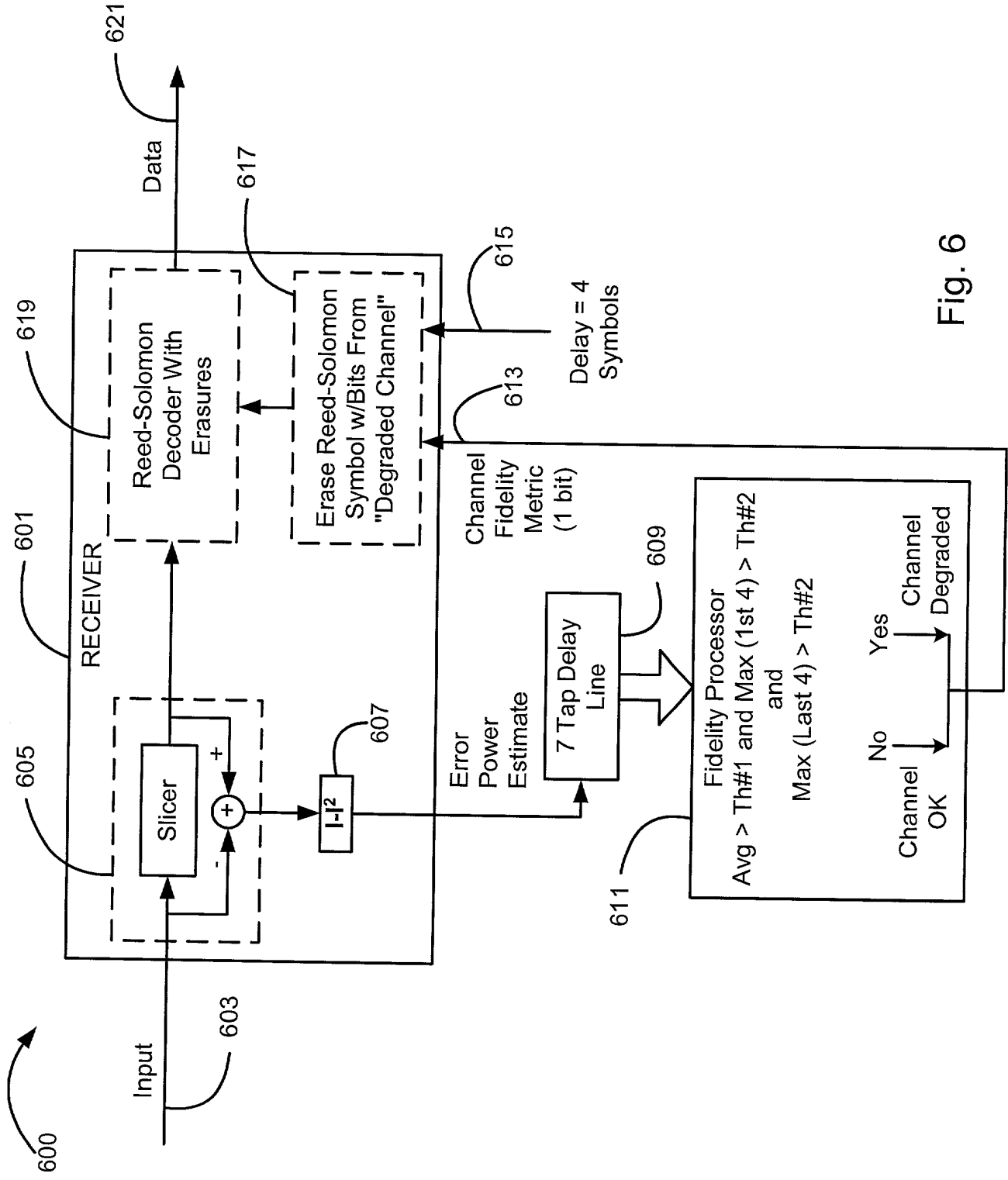


Fig. 6

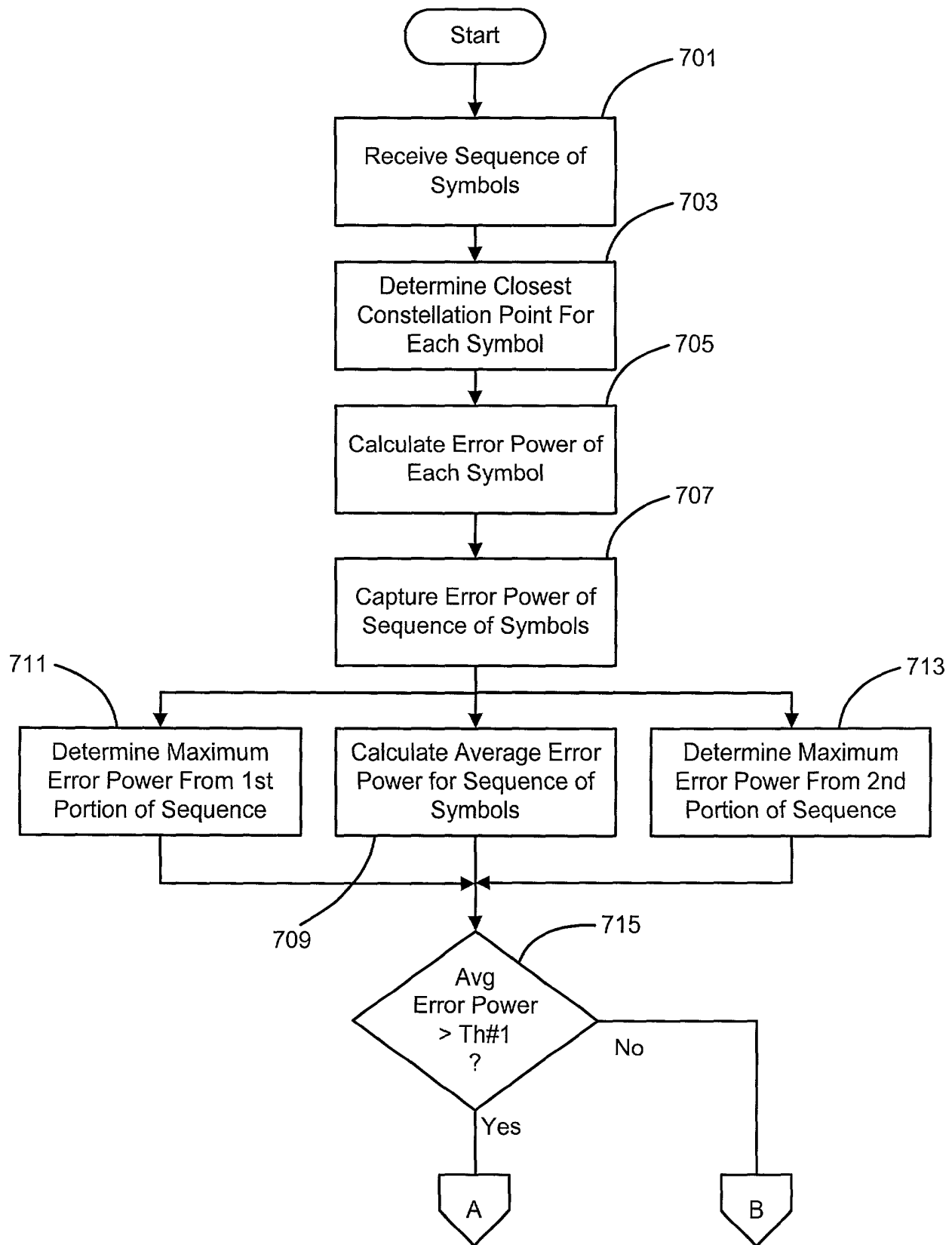


Fig. 7A

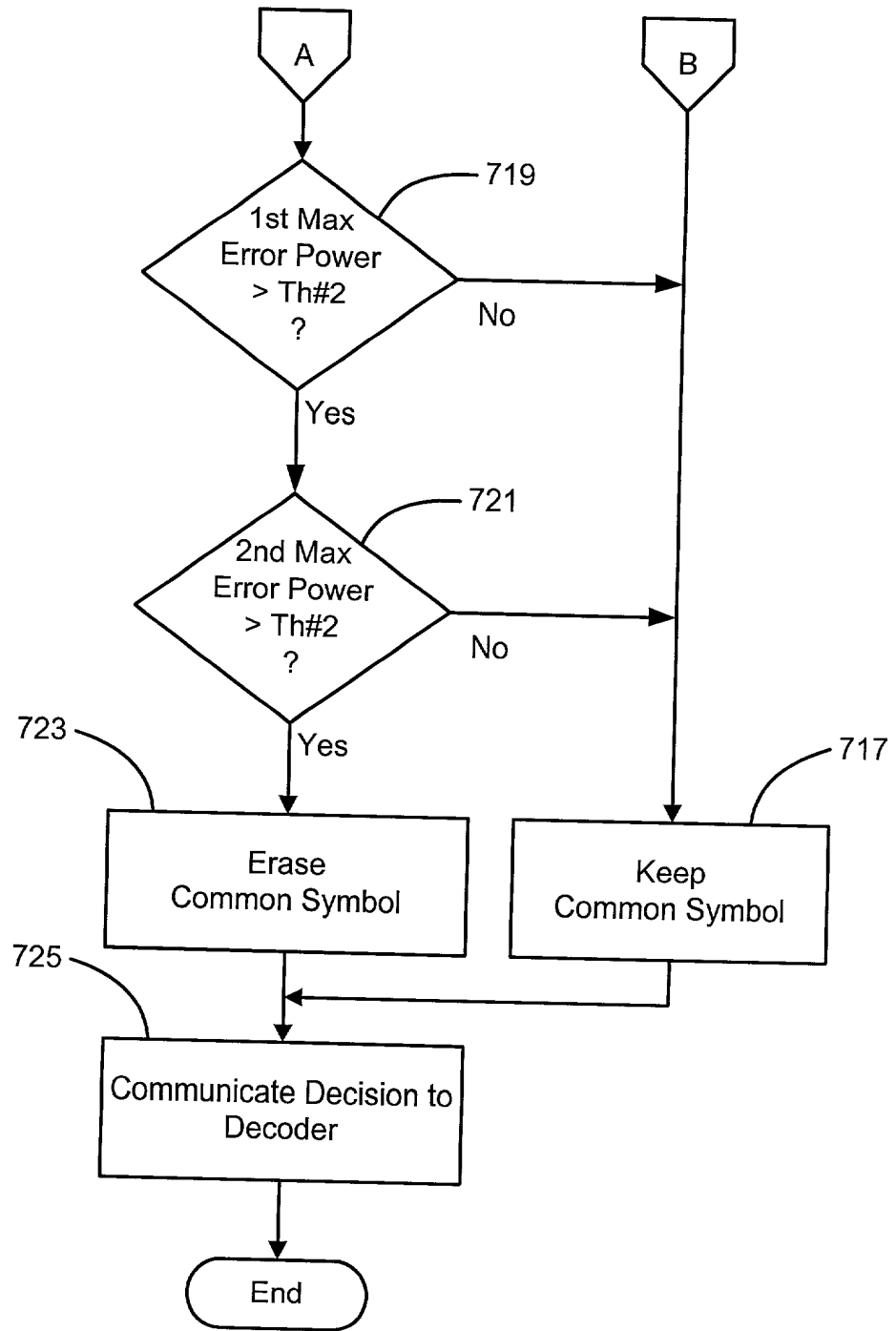


Fig. 7B



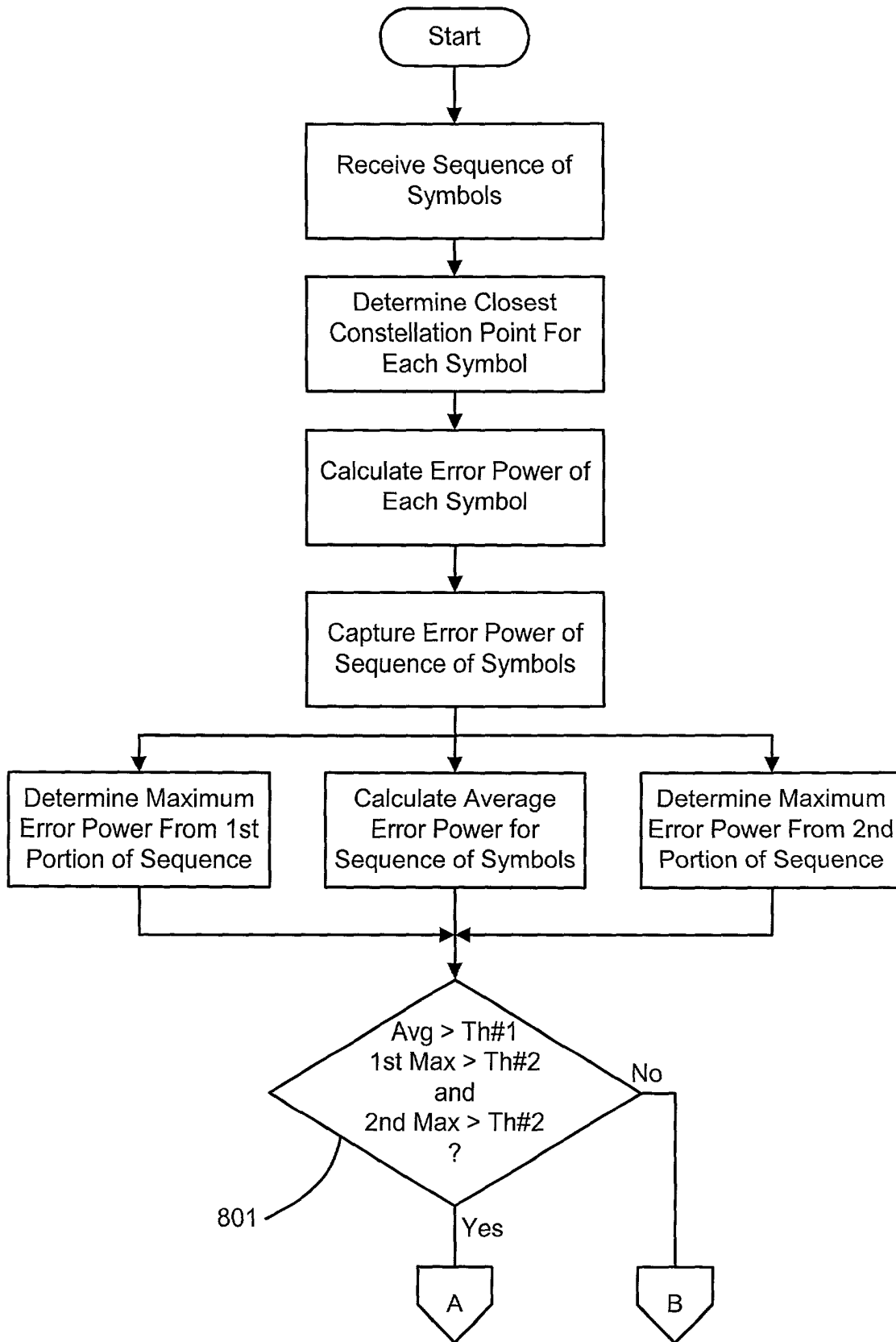


Fig. 8A

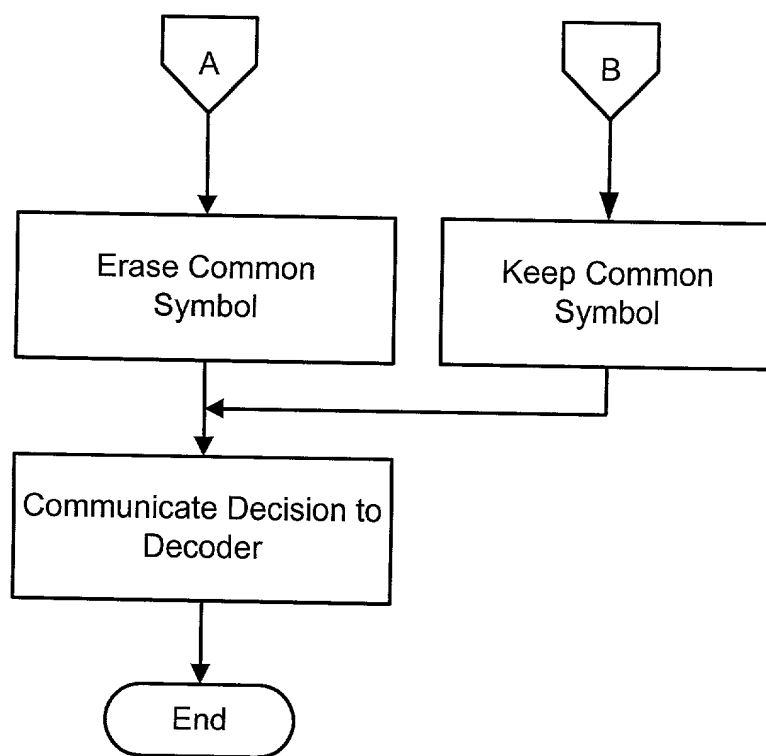


Fig. 8B

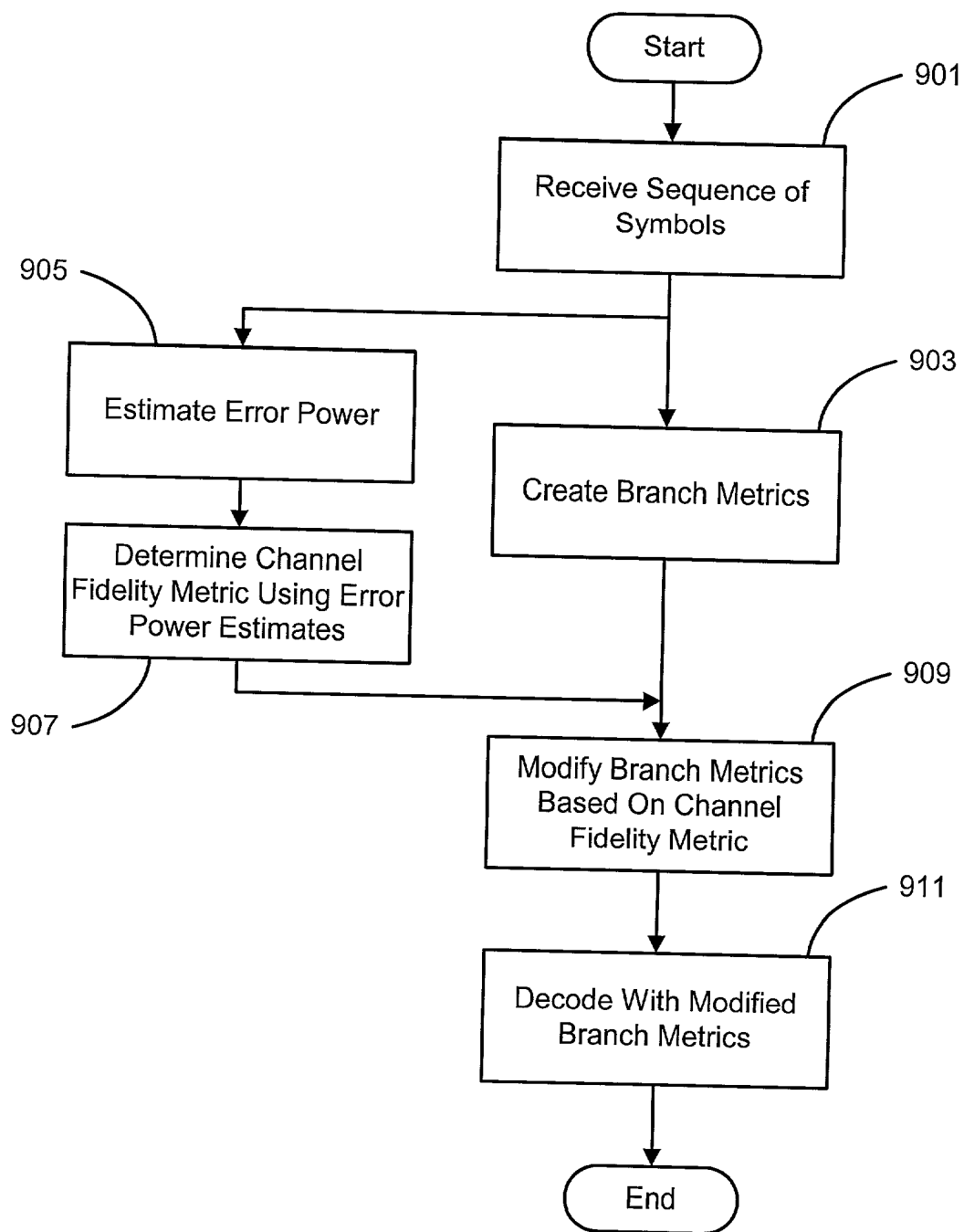


Fig. 9

FIG. 10 is a block diagram of a system 1000 for processing data. The system 1000 includes an input 1003, a delay block 1001, a normal receiver (hard and soft decisions) block 1005, two FEC decode blocks 1015 and 1017, an encode block 1007, an error estimate block 1009, an error power estimate block 1011, and a fidelity processor block 1013. The input 1003 is connected to the delay block 1001 and the normal receiver block 1005. The output of the delay block 1001 is connected to the first FEC decode block 1015. The output of the normal receiver block 1005 is connected to the second FEC decode block 1017. The output of the first FEC decode block 1015 is connected to the encode block 1007. The output of the second FEC decode block 1017 is connected to the error estimate block 1009. The output of the encode block 1007 is connected to the error power estimate block 1011. The output of the error power estimate block 1011 is connected to the fidelity processor block 1013. The output of the fidelity processor block 1013 is connected to the input 1003.

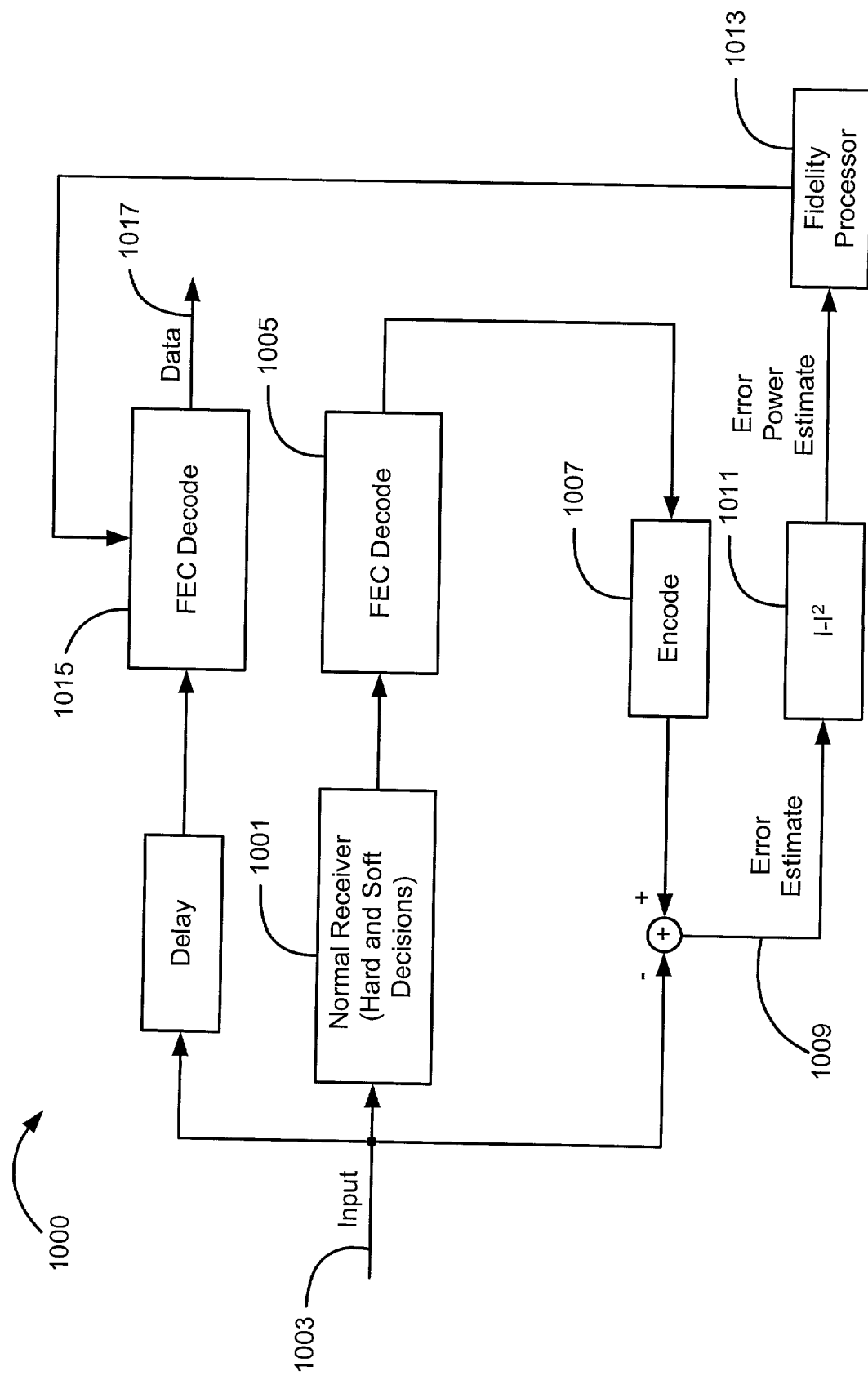


Fig.10

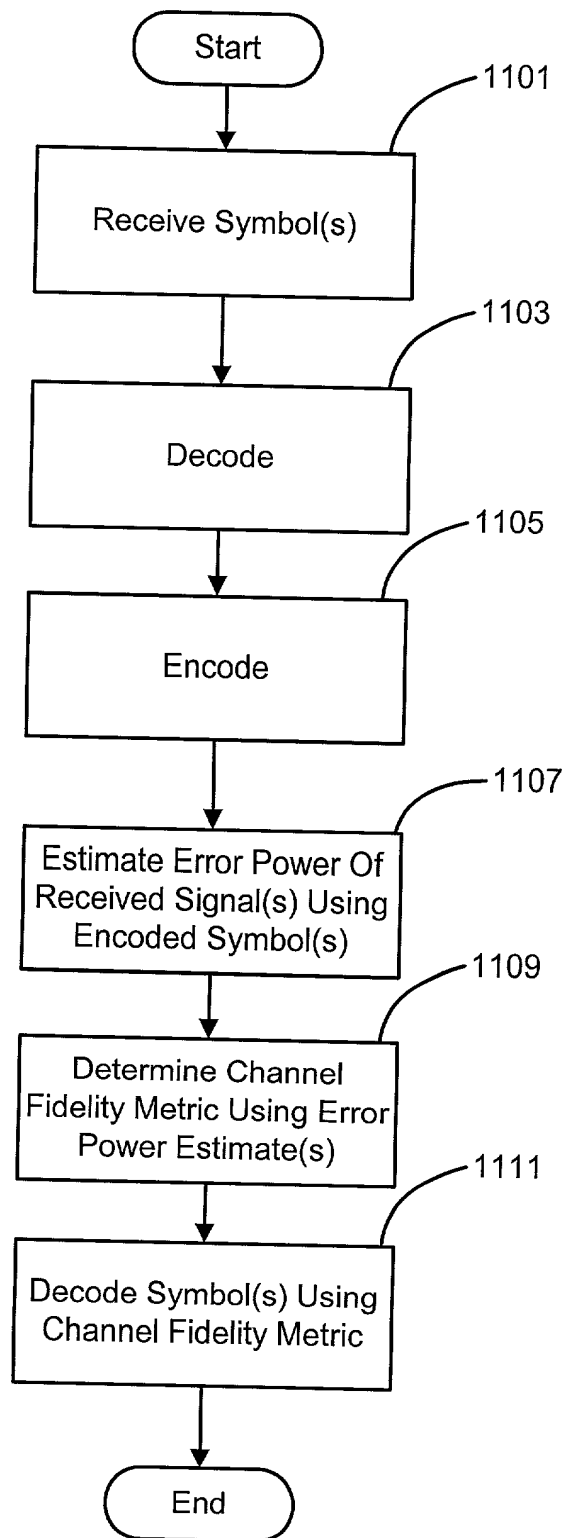


Fig. 11